I Number	Hits	Search Text	DB	Time stamp
1	126	(((bonding adj pad) or interconnect) same passivation same polyimide and etching) and @ad<="20010105"	USPAT; US-PGPUB	2002/07/30 13:36
2	1	("6287730").PN.	USPAT; US-PGPUB	2002/07/30 13:53
3	96	hardened with layer with polyimide	USPAT; US-PGPUB	2002/07/30 14:02
4	15	(hardened with layer with polyimide) same etching	USPAT; US-PGPUB	2002/07/30 13:54
5	8	hardened with layer with (surface near3 polyimide	USPAT; US-PGPUB	2002/07/30 14:09
6	6	hardened with layer with (surface near3 polyimide	EPO; JPO; DERWENT; IBM_TDB	2002/07/30 14:[illegible]
7	13	hardened with layer same (surface near3 polyimide	USPAT; US-PGPUB	2002/07/30 14:[illegible]
8	5	(hardened with layer same (surface near3 polyimide) not (hardened with layer with (surface near3 polyimide)	USPAT; US-PGPUB	2002/07/30 14:[illegible]
9	8	hardened with layer same (surface near3 polyimide	EPO; JPO; DERWENT; IBM_TDB	2002/07/30 14:13
10	2	hardened with layer same (surface near3 polyimide same etching	EPO; JPO; DERWENT; IBM_TDB	2002/07/30 14:13
11	4	hardened with layer same (surface near3 polyimide) same etching	USPAT; US-PGPUB	2002/07/30 14:43
12	1	hardened adj layer same polyimide same etching	USPAT; US-PGPUB	2002/07/30 14:44
13	1	hardened adj layer same polyimide same etching	EPO; JPO; DERWENT; IBM_TDB	2002/07/30 14:46
14	1	hardened adj layer same polyimide and etching	EPO; JPO; DERWENT; IBM_TDB	2002/07/30 14:46
15	3	hardened adj layer same polyimide and etching	USPAT; US-PGPUB	2002/07/30 14:47

TDB-ACC-NO: NN8504649B

DISCLOSURE TITLE: Multilayer Cleavage Technique

PUBLICATION-DATA: IBM Technical Disclosure Bulletin, April 1985, US

VOLUME NUMBER: 27

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PUBLICATION-DATE: April 1, 1985 (19850401)

CROSS REFERENCE: 0018-8689-27-11-6498

DISCLOSURE TEXT:

- Physical cleavage of semiconductor wafers having a **polyimide** layer, to expose an etched profile or step coverage over topography, is very difficult, and yields typically poor results. The **polyimide** does not break cleanly, but normally pulls and curls away from the cleaved edge, preventing inspection of the desired features. The following cleavage technique eliminates these problems since it does not require breaking of the wafers. The procedure is performed as follows: 1. The wafers which have the desired features to be inspected, e.g., coverage of **polyimide** over topography or an etched via hole profile, are coated with a photoresist layer whose thickness is about the same as the **polyimide** thickness. This step fills in all etched via holes and planarizes the wafer surface. The photoresist is baked at about 190 C. 2. The photoresist surface is etched in a

barrel plasma system using oxygen for about 5 minutes. This step was found to be essential for proper adhesion of the metal which will be deposited next. 3. Deposit about 5000 A of metal, aluminum or aluminum/copper, without substrate heat. 4. Coat the metal-covered surface with another photoresist layer, about 10,000 A thick. Prebake the photoresist and prepare for exposure. 5. Expose a pattern with numerous lines (such as a metal-level pattern) in the top photoresist layer, then develop and wet-etch the metal, leaving a large number of metal lines on the wafer. 6.

Etch through the photoresist and **polyimide** not covered by the metal lines using a reactive ion etch (RIE) with oxygen gas. This step will sever the **polyimide** vertically, permitting inspection of the topography when the photoresist and metal are later removed. The underlying film is plasma-enhanced nitride, which can be etched in the RIE using CF4 . It is important to note that neither the O2 plasma nor the CF4 plasma will chemically attack (etch) the metal; thus the aluminum serves as a perfect nonerodable etch mask. It is important that the cathode voltage on the RIE be kept low during the **etching** process -- about -150 volts or less; otherwise, physical sputtering of the metal will take place and obscure the final results. 7. After the **etching** is done, it is necessary to remove the metal and the planarizing photoresist.

This is accomplished by first using an O2 plasma in a barrel reactor for several minutes to

remove the CF4 **hardened layer** of the top surface of the photoresist.

(This is not necessary if CF4 was not used.) The photoresist and

metal are then removed by soaking in NMP as in normal lift-off

procedure. The wafers are now ready for inspection. The technique

provides vertical cleavage through features which repeat themselves

many times on a wafer and thus have a very good chance of being

coincident with the large number of metal cleavage edges available.

US-PAT-NO: 5807787

DOCUMENT-IDENTIFIER: US 5807787 A

TITLE: Method for reducing surface leakage current on semiconductor
integrated circuits during polyimide passivation

---------- KWIC ---------

In recent years photosensitive **polyimide** has attracted considerable interest as
the **passivation** coating over the bonding pads. These photosensitive polyimides
have the desirable properties of the more conventional polyimides, such as low
dielectric constants, relatively high temperature stability (up to about
450.degree. C.), planarizing properties, etc., but can also be patterned like
a photoresist mask, and then remain on the substrate to serve as the
passivation layer. This later attribute is highly desirable for reducing
manufacturing cost. Typically a photosensitive **polyimide** precursor is coated
on the substrate using, for example, conventional photoresist spin coating
techniques. The photosensitive **polyimide** precursor, after a low temperature
prebake, is then exposed through a photo-mask or reticle using, for example, a
step and repeat projection aligner and ultra violet (UV) radiation source. The
UV exposed portions of the **polyimide** precursor are crosslinked while leaving
unexposed regions over the bonding pads that are not crosslinked. During
development, the unexposed **polyimide** precursor regions over the bonding pads
are dissolved away providing openings over the **bonding pad** areas. Further
thermal curing yields a permanent **polyimide passivation**

layer which elsewhere
on the substrate. A schematic cross sectional view of a portion of this
bonding pad structure having the **passivation** layers is shown in FIG. 1. Shown
are two adjacent bonding pads 4 composed of metal such as aluminum (Al) or an
aluminium-copper alloy on a top insulating layer 10 which covers the
semiconductor integrated circuit. The contacts between the bonding pads and
the integrated circuit are not shown to simplify the drawing. The first
passivation layer 12 is deposited over the bonding pads and contact openings 6
are etched in the insulating layer 12 to the bonding pads. The photosensitive
polyimide passivation layer 14 is then spin-coated and patterned to provide
openings over the bonding pads, as shown in FIG. 1.

Like photoresist processing, when the **polyimide** is removed over the bonding
pads by dissolving away the non-crosslinked **polyimide, a polyimide** residue
remains that can result in unwanted electrical opens or high contact resistance
during testing and/or wire bonding. Typically a mild plasma ashing (plasma
descumming) step is performed in an oxygen plasma to insure that the trace
amounts of the **polyimide** residue are removed. Unfortunately, this plasma
ashing can also effect the first **passivation** layer making the surface
conductivity higher, and thereby resulting in significantly higher surface
leakage currents across the insulating layer 12 (see FIG. 1) between the
bonding pads 4. As semiconductor devices are further reduced in size and the
circuit density increased, it will become even more important to minimize
leakage currents to maintain circuit performance. Also, with further increase
in circuit density and increasing I/O count on the chip the **bonding pad** pitch

will further decrease. Therefore, there is an increasing need in the semiconductor industry to minimize the leakage currents on the integrated circuit.

The method starts by providing a semiconductor substrate on which are already formed the necessary discrete semiconductor devices, such as field effect transistors (FET's), bipolar transistor and similar devices. A multilayer of patterned conducting layers, such as doped polysilicon, silicides and metal with interposed insulating layers, such as chemical vapor deposited silicon oxides, are used to electrically **interconnect** the device, and thereby form the integrated circuit. The number of metal levels can vary depending on the circuit design, but are typically between about 2 to 4 layers. A top insulating layer, such as a silicon oxide, is provided with contact openings or via holes to the appropriate regions of the integrated circuit to which the input/out signals and the power and ground plane contacts are to be made. An array of electrically conducting bonding pads are then formed over the contact openings to provide the external wiring contacts for the single or multi-chip carrier. Typically the bonding pads are composed of aluminium or aluminium/copper alloys. Alternatively, aluminum/silicon and aluminum/copper/silicon alloys can also be utilized for making the bonding pads. A first **passivation** layer, typically a low temperature oxide, such as a plasma enhanced CVD oxide, is deposited over the bonding pads and openings are formed in the first **passivation** layer to the bonding pads. A much thicker second **passivation** layer, composed of a photosensitive **polyimide,** is deposited by spin coating a photosensitive **polyimide** precursor which

is then exposed with ultra violet (UV) radiation through a mask to crosslink the **polyimide**. The **polyimide** regions over the bonding pads and over the first **passivation** layer between the bonding pads is masked from UV exposure (crosslinking) and is dissolved away. Conventional plasma ashing in oxygen (O_2) is then performed to remove trace amounts of **polyimide** residue from the bonding pads for minimizing contact electrical resistance. This ashing, unfortunately, increases the surface electrical conductivity on the first **passivation** layer between the bonding pads and thereby increases the surface leakage currents by about an order of magnitude. By the method of this invention, the substrate is thermally treated in air or nitrogen ambient which reduces the leakage current back to the previous values before the plasma ashing. This provides a **polyimide passivation** layer with improved (lower) surface leakage currents than the conventional process without the thermal treatment.

FIG. 1 is a schematic cross sectional view of a portion of a typical **bonding pad** area depicting the exposure of the photosensitive **polyimide passivation** layer using UV radiation and mask.

With continued down scaling of the semiconductor devices dimensions, the device parametric operating parameters, such as voltage and current, are also reduced, and therefore, it is very important to minimize the leakage currents in the circuit. In particular, it is important to maintain a low surface leakage current on the surface of the first **passivation** layer 12 between the adjacent bonding pads 4. However, in conventional processing after forming the bonding pads, a thick **polyimide** layer is typically used to passivity the integrated

circuit from contamination and damage. A plasma ashing step is then required to remove residual **polyimide** over the **bonding pad** that would otherwise degrade the electrical contact during testing and wire bonding. Although the plasma ashing improves the electrical contact it is also known to effect the exposed **passivation** layer 12 between the bonding pads 4 results in excessive surface leakage currents between pads, as depicted in FIG. 1 by the double headed arrow 1.

As shown in FIG. 2, the opaque portion 18 of the mask 19 over the **bonding pad** areas prevent the UV radiation 20 from crosslinking the photosensitive **polyimide** precursor layer 14', and therefore, is dissolved away in the developer while the crosslinked regions 14 remains as the second **passivation** layer 14 on the substrate, as shown in FIG. 1.

	U	1 [1]	Document ID	Issue Date	Pages
1	☐	☐	US 20020076913 A1	20020620	10
2	☐	☐	US 20020064929 A1	20020530	15
3	☐	☐	US 6410414 B1	20020625	9
4	☐	☐	US 6413468 B1	20011106	15
5	☐	☐	US 6306342 B1	20011016	22
6	☐	☐	US 6303434 B1	20011009	10
7	☐	☐	US 6184067 B1	20010904	12
8	☐	☐	US 6208753 B1	20010508	5
9	☐	☐	US 6143638 A	20001107	15
10	☐	☐	US 6046107 A	20000516	5
11	☐	☐	US 5986335 A	19991116	34
12	☐	☐	US 5980025 A	19991109	6
13	☐	☐	US 5824234 A	19981020	8
14	☐	☐	US 4978419 A	19901218	5

	Title	Current OR	Current XRef
1	SEMICONDUCTOR DEVICE RESISTANT TO SOFT ERRORS AND A METHOD FOR MANUFACTURING THE SEMICONDUCTOR DEVICE	438/614	438/611
2	NOVEL PASSIVATION STRUCTURE AND ITS METHOD OF PASSIVATION	438/612	
3	Method for fabricating a semiconductor device	438/612	438/11; 438/16; 438/29
4	Method for fabricating an electrically addressable silicon-on-sapphire light valve	438/30	438/149; 438/150
5	Method for forming high performance system-on-chip using post passivation process	438/238	438/239; 438/381; 438/393; 438/761
6	Process for forming an electrical device	438/612	438/[illegible]
7	Non-metallic barrier formation for copper damascene type interconnects	438/687	438/[illegible]; [illegible]
8	Method of fabricating a bonding pad structure for improving the bonding pad surface quality	438/612	438/[illegible]; 438/[illegible]
9	Passivation structure and its method of fabrication	438/612	438/[illegible]; 438/612; 438/623
10	Surface treatment for bonding pad	134/2	134/26; 438/118; 438/[illegible]
11	Semiconductor device having a tapeless mounting	257/668	257/[illegible]; 257/[illegible]; 257/[illegible]
12	Thermal inkjet printhead with increased resistance control and method for making the printhead	347/62	29/890.1
13	Method for forming low contact resistance bonding pad	216/18	216/[illegible]; 216/[illegible]; 216/78; 438/700
14	Process for defining vias through silicon nitride and polyamide	438/701	438/640; 438/713; 438/724; 438/725

	Retrieval Classif	Inventor	S	C	P	2	3	4	5
1		LEE, JOO-HERN	☒	☐	☐	☐	☐	☐	☐
2		BOHR, MARK T.	☐	☐	☐	☐	☐	☐	☐
3		Lee, Joo-hern	☐	☐	☐	☐	☐	☐	☐
4		Shimabukuro, Randy L. et al.	☐	☐	☐	☐	☐	☐	☐
5		Lin, Mou-Shiung	☐	☐	☐	☐	☐	☐	☐
6		Flynn, Todd M. et al.	☐	☐	☐	☐	☐	☐	☐
7		Chodi, Simon et al.	☐	☐	☐	☐	☐	☐	☐
8		Lo, Yung-Tsun et al.	☐	☐	☐	☐	☐	☐	☐
9		Bohr, Mark T.	☐	☐	☐	☐	☐	☐	☐
10		Yu, Chia-Chieh et al.	☐	☐	☐	☐	☐	☐	☐
11		Amagai, Masazumi	☐	☐	☐	☐	☐	☐	☐
12		Burke, Cathie J. et al.	☐	☐	☐	☐	☐	☐	☐
13		Jou, Chen-Shin et al.	☐	☐	☐	☐	☐	☐	☐
14		Nanda, Madan M. et al.	☐	☐	☐	☐	☐	☐	☐

	Image Doc. Displayed	PT
1	US 20020076913	☐
2	US 20020064929	☐
3	US 5410614	☐
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12	US 5980025	☐
13	US 5824234	☐
14	US 4978419	☐

	U	1 [1]	Document ID	Issue Date	Pages
15	☐	☐	US 4927505 A	19900522	5
16	☐	☐	US 4827326 A	19890502	5

	Title	Current OR	Current XRef
15	Metallization scheme providing adhesion and barrier properties	205/123	204/192.25; 204/192.3; 205/135; 257/781; 42[illegible]/620; [illegible]/614; [illegible]/653; [illegible]/754
16	Integrated circuit having polyimide/metal passivation layer and method of manufacture using metal lift-off	257/759	2[illegible]/13; 2[illegible]/48; 25[illegible]/774; 43[illegible]/313; 43[illegible]/317; 43[illegible]/612; 43[illegible]/670; 43[illegible]/951

	Retrieval Classif	Inventor	S	C	P	2	3	4	5
15		Sharma, Ravinder K. et al.	☒	☐	☐	☐	☐	☐	☐
16		Altman, Leonard F. et al.	☒	☐	☐	☐	☐	☐	☐

L Number	Hits	Search Text	DB	Time Stamp
5	6803	(bonding adj pad) or interconnect and passivation and polyimide and etching	USPAT; US-PGPUB	2002/10/30 10:11
6	149	((bonding adj pad) or interconnect same passivation same polyimide and etching	USPAT; US-PGPUB	2002/10/30 10:21
7	126	((bonding adj pad) or interconnect same passivation same polyimide and etching) and @ad<=20010105	USPAT; US-PGPUB	2002/10/30 10:22

US-PAT-NO: 6403449

DOCUMENT-IDENTIFIER: US 6403449 B1

TITLE: Method of relieving surface tension on a semiconductor wafer

---------- KWIC ---------

After forming the passivation layer, a protective polyimide layer can be formed to function as a die coat which protects the passivation layers from cracking, for example from contact with a lead frame in a "leads-over-chip" assembly. The polyimide material can comprise an organic material spun onto the wafer surface. A polyimide which is sensitive to ultraviolet light can be used or, in the alternative, a UV-sensitive resist is patterned over the polyimide to expose the bond pads. The polyimide (or the resist) is exposed to a patterned UV source, and the polyimide is etched from the bond pads and any other necessary locations such as fuse banks. A negative resist/polyimide can also be used. After **etching** the polyimide from the bond pads and other areas, a final cure of the polyimide is performed, for example by exposing the polyimide to a temperature of from about 200.degree. C. to about 310.degree. C. for a period of about 9 hours. This step drives out solvents from the **polyimide** and reduces the **layer** thickness from about 14 microns to about 9 microns and leaves a **hardened** film.

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hardened <near/1> layer <paragraph> polyimide

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No.	Database	Search term	Info added since	Results	
1	INZZ	hardened NEAR layer WITH polyimide	unrestricted	0	-
2	INZZ	hardened WITH layer WITH polyimide	1980	0	-
3	INZZ	hardened WITH layer AND polyimide	1980	0	-
4	INZZ	hardened WITH layer AND polyimide	19700101	0	-

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